WHAT IS CLAIMED IS:

1. A controller for a memory system, said controller coupled to a data strobe bus, to an interconnect, and to a clock bus, said controller comprising:

an output buffer configured to assert a first data strobe signal on the data strobe bus when said output buffer is enabled, said first data strobe signal generated by the controller;

a register configured to store information representing a mode of controller operation, the output buffer enabled during transfers from the controller of a first data signal over the interconnect when said mode of controller operation is set to a first mode of controller operation, the output buffer continuously enabled when said mode of controller operation is set to a second mode of controller operation; and

the controller configured to receive a clock signal over the clock bus, said controller further configured to clock receipt of a second data signal over the interconnect with said clock signal.

2. The controller of claim 1, wherein the controller is configured to adjust, when the mode of controller operation is set to the second mode of controller operation, a phase of the clock signal in accordance with a pre-existing calibration while receiving the second data signal over the interconnect.

3. The controller of claim 1, wherein the controller is configured to use, when the mode of controller operation is set to the first mode of controller operation, a second data strobe signal remotely asserted on the data strobe bus as a phase reference while receiving the second data signal over the interconnect.

4. The controller of claim 1, further comprising:

a circuit configured to receive as a first input a mode of controller operation from the register, said first input at a first logic level when said mode of controller operation is set to the first mode of controller operation and said first input at a second logic level when said mode of controller operation is set to the second mode of controller operation;

the circuit configured to receive as a second input an operational state of said controller, said operational state set to the second logic level during the transfers of the first data signal over the interconnect from the controller; and

an output of the circuit coupled to the output buffer such that said output buffer is enabled by said circuit when either the first input or the second input is set to the second logic level.

5. A method of operating a memory system controller, comprising:

maintaining a mode of controller operation;

generating a first data strobe signal;

enabling, when the mode of controller operation is set to a first mode of controller operation, transmission of the first data strobe signal while transferring a first data signal;

enabling, when the mode of controller operation is set to a second mode of controller operation, continuous transmission of the first data strobe signal;

receiving a clock signal; and

clocking receipt of a second data signal with a reference signal.

6. The method of claim 5, further comprising:

adjusting, when the mode of controller operation is set to the second mode of controller operation, a phase of the clock signal in accordance with a pre-existing calibration so as to generate the reference signal while receiving the second data signal.

7. The method of claim 5, further comprising:

using, when the mode of controller operation is set to the first mode of controller operation, a second data strobe signal remotely transmitted by a memory device as the reference signal, and using the reference signal as a phase reference while receiving the second data signal.

8. A memory device to store data in a memory system, the memory device coupled to a data strobe bus, an interconnect, and a clock bus, wherein

the memory device is configured to receive over the data strobe bus a data strobe signal continuously, remotely asserted on said data strobe bus;

the memory device is configured to receive over the interconnect a first data signal in conjunction with the data strobe signal, said memory device further configured to clock receipt of said first data signal with the data strobe signal;

the memory device is configured to receive over the clock bus a clock signal; and

the memory device is configured to transmit over the interconnect a second data signal in conjunction with the clock signal, said memory device further configured to clock transmission of said second data signal with the clock signal.

9. A method of operating a memory device to store data in a memory system, comprising:

receiving a continuous data strobe signal;

intermittently receiving a first data signal in conjunction with the continuous data strobe signal;

clocking receipt of the first data signal with the data strobe signal;

receiving a clock signal;

intermittently transmitting a second data signal in conjunction with the clock signal; and

clocking transmission of the second data signal with the clock.

10. A memory device to store data in a memory system, the memory device coupled to a data strobe bus, an interconnect, and a clock bus, wherein

the memory device is configured to receive over the data strobe bus a data strobe signal continuously, remotely asserted on said data strobe bus;

the memory device is configured to receive over the interconnect a first data signal in conjunction with the data strobe signal, said memory device further configured to clock receipt of said first data signal with the data strobe signal; and

the memory device is configured to transmit over the interconnect a second data signal in conjunction with the data strobe signal, said memory device further configured to clock transmission of said second data signal with the data strobe signal.

11. A method of operating a memory device to store data in a memory system, comprising

receiving a continuous data strobe signal;

intermittently receiving a first data signal for storage in conjunction with the continuous data strobe signal;

clocking receipt of the first data signal with the data strobe signal;

intermittently transmitting from storage a second data signal in conjunction with the data strobe signal; and

clocking transmission of the second data signal with the data strobe signal.

12. A memory device to store data in a memory system, the memory device coupled to a data strobe bus and an interconnect, said memory device comprising:

an output buffer configured to transmit a first data strobe signal when enabled;

circuitry to transmit over the interconnect a first data signal, said first data signal transmitted in conjunction with the first data strobe signal when the output buffer is enabled;

a register to store a mode of memory device operation, the memory device configured to enable the output buffer when said mode of memory device operation is set to a first mode of memory device operation, the memory device configured to disable the output buffer when said mode of memory device operation is set to a second mode of memory device operation; and

additional circuitry configured to receive over the interconnect a second data signal in conjunction with a second data strobe signal remotely asserted on the data strobe bus, said second data strobe signal clocking receipt of said second data signal.

13. A method of operating a memory device to store data in a memory system, comprising

intermittently receiving a first data signal in conjunction with a first data strobe signal, said first data strobe signal clocking receipt of said first data signal;

intermittently transmitting a second data signal;

storing a mode of memory device operation;

setting an output to a second data strobe signal while transmitting the second data signal when the stored mode of memory device operation is a first mode of memory device operation; and

preventing output of the second data strobe when the mode of memory device operation is set to a second mode of memory device operation.

14. A memory device to store data in a memory system, the memory device coupled to a data strobe bus, an interconnect, a clock bus, and a control and address bus, wherein

the memory device is configured to receive over the control and address bus a control and address signal in conjunction with a clock signal remotely asserted on the clock bus, said clock signal clocking receipt of said control and address signal;

the memory device is configured to receive over the interconnect a first data signal in conjunction with a first data strobe signal remotely asserted on the data strobe bus, said first data strobe signal clocking receipt of said first data signal; and

the memory device is configured to transmit over the interconnect a second data signal, the first data strobe signal clocking transmission of said second data signal.

15. A method of operating a memory device to store data in a memory system, comprising:

intermittently receiving a control and address signal in conjunction with a clock signal, said clock signal clocking receipt of said control and address signal;

intermittently receiving a first data signal in conjunction with a first data strobe signal, said first data strobe signal clocking receipt of said first data signal;

intermittently transmitting from storage a second data signal, said first data strobe signal clocking transmission of said second data signal.

16. A memory device to store data in a memory system, the memory device coupled to a data strobe bus, an interconnect, and a clock bus, wherein

the memory device is configured to receive over the interconnect a first data signal in conjunction with a first data strobe signal remotely asserted on the data strobe bus, said first data strobe signal providing a phase reference while receiving said first data signal; and

the memory device includes a register to store a reference mode;

the memory device is configured to receive over the clock bus a clock signal;

the memory device is configured to transmit over the interconnect a second data signal;

the memory device is configured to use, when the reference mode is set to a first reference mode, the first data strobe signal as a phase reference while transmitting the second data signal; and

the memory device is configured to use, when the reference mode is set to a second reference mode, the clock signal as the phase reference while transmitting the second data signal.

17. A method of operating a memory device to store data in a memory system, comprising

intermittently receiving a first data signal in conjunction with a remotely asserted first data strobe signal, said first data strobe signal providing a phase reference while receiving said first data signal;

storing a reference mode;

receiving a clock signal;

intermittently transmitting a second data signal;

using, when the reference mode is set to a first reference mode, the first data strobe signal as a phase reference while transmitting the second data signal; and

using, when the reference mode is set to a second reference mode, the clock signal as the phase reference while transmitting said second data signal.

18. A memory system, comprising

a controller, a memory device, and a clock signal generator;

a data strobe bus coupling the controller to the memory device;

an interconnect coupling the controller to the memory device;

the clock signal generator configured to transmit a clock signal to the controller;

the controller configured to use the clock signal in conjunction with a pre-existing calibration to clock a first data signal received from the memory device over the interconnect;

the controller further configured to continuously assert a data strobe signal on the data strobe bus; and

the memory device configured to use the data strobe signal to clock a second data signal received from the controller over the interconnect.

19. The memory system of claim 18, wherein the calibration comprises a delay to offset state transitions of the clock signal that otherwise time sampling of the first data signal by the controller.

20. The memory system of claim 18, wherein the memory device is further configured to use the data strobe signal as a phase reference while transmitting the second data signal.

21. The memory system of claim 18, wherein

the clock signal generator is further configured to transmit the clock signal to the memory device; and

the memory device is further configured to use the clock signal as a phase reference while transmitting the second data signal.

22. A controller for a memory system, said controller coupled to a data strobe bus, to an interconnect, and to a clock bus, said controller comprising:

a bimodal data strobe interface configured to connect the controller to the data strobe bus; and

means for storing information representing a mode of controller operation;

wherein the bimodal data strobe interface includes means for utilizing the data strobe bus as a unidirectional data strobe bus when the mode of controller operation is set to a first mode and for utilizing the data strobe bus as a bidirectional data strobe bus when the mode of controller operation is set to a second mode.

23. A controller for a memory system, said controller coupled to a data strobe bus, to an interconnect, and to a clock bus, said controller comprising:

means for asserting a first data strobe signal on the data strobe bus when said asserting means is enabled;

means for storing information representing a mode of controller operation;

wherein the asserting means is enabled during transfers from the controller of a first data signal over the interconnect when said mode of controller operation is set to a first mode of controller operation, and wherein the asserting means is continuously enabled when said mode of controller operation is set to a second mode of controller operation; and

the controller configured to receive a clock signal over the clock bus, said controller further configured to clock receipt of a second data signal over the interconnect with said clock signal.

24. A memory device to store data, the memory device coupled to a data strobe bus, an interconnect, and a clock bus, the memory device comprising:

a bimodal data strobe interface configured to connect the memory device to the data strobe bus; and

a storage circuit for storing information representing a mode of operation;

wherein the bimodal data strobe interface includes means for utilizing the data strobe bus as a unidirectional data strobe bus when the mode of operation is set to a first mode and for utilizing the data strobe bus as a bidirectional data strobe bus when the mode of operation is set to a second mode.

25. A memory module, comprising:

a plurality of dynamic memory random access memory devices (DRAMs); and

a serial presence device configured to store information indicating whether the memory devices are bimodal with respect to use of a set of data strobe busses, wherein each of the memory devices, if bimodal, includes a configuration mechanism for configuring the memory device to drive a respective data strobe bus while transmitting data in one mode of operation and for configuring the memory device to not drive the data strobe bus while transmitting data in another mode of operation.